What is claimed is:

1. A test socket for a semiconductor device having a plurality of pins, the test socket comprising:

a body for receiving a semiconductor device, the body having an integrally formed guidepost and a chamfered impact base;

a floating base disposed within the body, floating base coming into contact with the semiconductor device and providing movement of the semiconductor device to alleviate unwanted pressure from the plurality of pins;

a plurality of pogo-pins adjacent to one another, each pogo-pin comprising a cylindrical chamber and a plunger having a crown top at both ends, one end for directly contacting a pin of the semiconductor device and the other end for contacting external test equipment; and

a back panel removably attached to the body.

2. The test socket of Claim 1 wherein the semiconductor device is Quad Flat Pack (QFP).

3. The test socket of Claim 1 wherein the guide post comprises:

a first portion having a substantially rectangular shape, a top edge, and a first side; and

a second portion having a substantially triangular shape and having a first leg at a ninety degree angle to a second leg, the first leg integrally connected to the first portion along its first side.

4. The test socket of Claim 1 wherein the chamfered impact base extends at an angle between zero and seven degrees below the horizontal axis of the crown top of the plurality of pogo pins.

5. The socket of Claim 1 wherein the floating base comprises:

a spring comprised of metallic material; and

a base component comprised of plastic material, the base component substantially square in shape and having a cylindrical shaft underneath to receive the spring.

6. The test socket of Claim 5 wherein the metallic material is a steel alloy.

7. The test socket of Claim 1 wherein the back panel has through holes to receive the plurality of pogo-pins.

8. The test socket of Claim 7 wherein screws are utilized to attach the back panel to the body.

9. The test socket of Claim 1 wherein the plurality of pogo-pins each comprise a plunger and an internal spring exerting a force upon the plunger at both ends.

10. The test socket of Claim 9 wherein the internal spring of each pogo-pin is disposed within the chamber of the pogo-pin.

11. The test socket of Claim 1 wherein the plurality of pogo-pins are comprised of metallic material.

12. The test socket of Claim 1 wherein the plurality of pogo-pins are plated with a metallic material.

13. The test socket of Claim 11 wherein the metallic material is gold.

14. The test socket of Claim 1 wherein the plurality of pogo-pins are sets of two pogo-pins for contacting each pin of the semiconductor device.

15. The test socket of Claim 1 wherein the guidepost includes a slanted groove for ensuring proper alignment of the semiconductor device.

16. The test socket of Claim 1 wherein the crown of the each of the plurality of pogo-pins comprises four pointed ends and a series of crevices for making contact with the pins of the semiconductor device.

17. The test socket of Claim 16 wherein the four pointed ends have a maximum pitch of 0.14mm.

18. A semiconductor device comprising:

a package;

an integrated circuit disposed within the package; and

a plurality of pins each having a series of contact marks, each set of contact marks being of substantially the same pattern and spaced by a predetermined pitch.

19. The semiconductor device of Claim 17 wherein a series of sets of contact marks result from the testing of the semiconductor device in a test socket comprising a plurality of pogo-pins having a crown portion with pointed ends for directly contacting the plurality of the semiconductor device, the pointed ends having the predetermined pitch.

20. The semiconductor device of Claim 20 wherein the predetermined pitch is less or equal to 0.14mm.

21. A method of testing a semiconductor device having a plurality of pins, the method comprising:

providing a test socket having a body for receiving a semiconductor device, the test socket including a plurality of guidepost integrally formed within the body and a plurality of pogo-pins adjacent to one another for directly contacting the plurality of pins;

aligning the semiconductor device within the body utilizing the guide posts;

applying a pressure which brings the plurality of semiconductor device pins into contact with the plurality of pogo-pins; and

testing the semiconductor device.

22. The method of Claim 21 wherein each of the plurality of pogo-pins comprises an internal spring disposed in a chamber, the internal spring utilized for evenly distributing pressure on the plurality of pogo-pins.